PRELIMINARY

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TFT MONOCHROME LCD MODULE

NL204153BM21-01

54cm (21.3 Type)

QXGA

PRELIMINARY DATA SHEET

DOD-PD-0418 (6th edition)

This PRELIMINARY DATA SHEET is updated document from DOD-PD-0246(5).

All information is subject to change without notice. Please confirm the sales representative before starting to design your system.

INTRODUCTION

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Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Military systems, aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems (medical equipment, etc.) and any other equipment

The quality grade of this product is ***"Standard"*** unless otherwise specified in this document. If customers intend to use this product for applications other than those specified for ***"Standard"*** quality grade, they should contact NEC sales representative in advance.

CONTENTS

1. OUTLINE

1.1 STRUCTURE AND PRINCIPLE

Monochrome LCD module NL204153BM21-01 is composed of the amorphous silicon thin film transistor liquid crystal display (a-Si TFT LCD) panel structure with driver LSIs for driving the TFT (Thin Film Transistor) array and a backlight.

The a-Si TFT LCD panel structure is injected liquid crystal material into a narrow gap between the TFT array glass substrate and a monochrome-filter glass substrate.

Grayscale data signals from a host system (e.g. PC, signal generator, etc.) are modulated into best form for active matrix system by a signal processing board, and sent to the driver LSIs which drive the individual TFT arrays.

The TFT array as an electro-optical switch regulates the amount of transmitted light from the backlight assembly, when it is controlled by data signals. Monochrome images are created by regulating the amount of transmitted light through the TFT array.

1.2 APPLICATION

- Monochrome monitor system

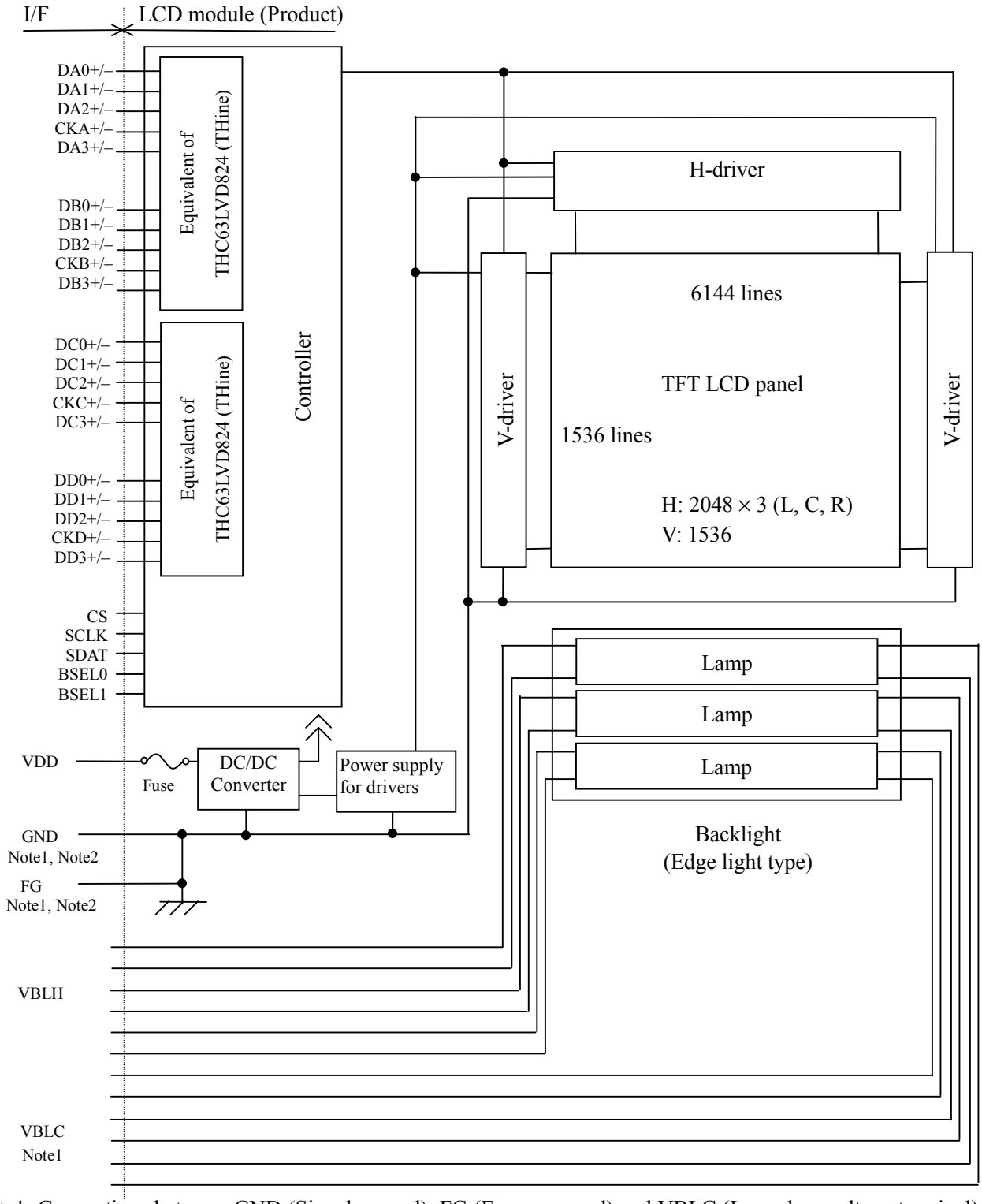
1.3 FEATURES

- Ultra-wide viewing angle (with lateral electric field)
- High luminance
- High contrast
- Low reflection
- High resolution
- 256 gray scale per 1 dot (8-bit)
- 4 ports LVDS interface
- Adjustable gamma characteristics by using built-in 10-bit LUT (look up table)
- Selectable LVDS data input map
- Small foot print
- Incorporated edge light type backlight (without inverter)

2. GENERAL SPECIFICATIONS

Display area	433.152 (H) × 324.864 (V) mm (typ.)	
Diagonal size of display	54 cm (21.3 inches)	
Drive system	a-Si TFT active matrix	
Display grayscale	256 gray scale per 1 dot (8-bit) (1 pixel consists of 3 dots (766 gray scale).)	
Pixel	2,048 (H) × 1,536 (V) pixels	
Pixel arrangement	Sub-pixel vertical stripe	
Dot pitch	0.0705 (H) × 0.2115 (V) mm	
Pixel pitch	0.2115 (H) × 0.2115 (V) mm	
Module size	457.0 (W) × 350.0 (H) × 25.0 (D) mm (typ.)	
Weight	3,800 g (typ.)	
Contrast ratio	700:1 (typ.)	6
Viewing angle	*At the contrast ratio ≥ 10:1* • Horizontal: Right side 85° (typ.), Left side 85° (typ.) • Vertical: Up side 85° (typ.), Down side 85° (typ.)	
Designed viewing direction	Viewing angle with optimum grayscale (γ=DICOM): normal axis	6
Polarizer surface	Antiglare	
Polarizer pencil-hardness	2H (min.) [by JIS K5400]	
Response time	*Ton+Toff (10%←→ 90%)* (35) ms (typ.)	6
Luminance	*At IBL= 6.0mArms / lamp* 800 cd/m^2 (typ.)	
Signal system	4 ports LVDS interface (THC63LVD824×2 pcs, THine Electronics, Inc. or equivalent) LCR 8-bit signals, Data enable signal (DE), Dot clock (CLK)	
Power supply voltage	LCD panel signal processing board: 12.0V	
Backlight	Edge light type: 6 cold cathode fluorescent lamps (without inverter)	
Power consumption	*At checkered flag pattern and IBL= 6.0mArms / lamp* 34.2 W (typ.)	

3. BLOCK DIAGRAM



Note1: Connections between GND (Signal ground), FG (Frame ground) and VBLC (Lamp low voltage terminal) in the LCD module

GND - FG	Connected
GND - VBLC	Not connected
FG - VBLC	Not connected

Note2: GND and FG must be connected to customer equipment's ground, and it is recommended that GND, FG and customer inverter ground are connected together in customer equipment.

4. DETAILED SPECIFICATIONS

4.1 MECHANICAL SPECIFICATIONS

Parameter	Specification	Unit
Module size	457.0 ± 0.5 (W) × 350.0 ± 0.5 (H) ×25.0±0.5 (D) Note1	mm
Display area	433.152 (W) × 324.864 (H) Note1	mm
Weight	3,800 (typ.), 4,000 (max.)	g

Note1: See "**7. OUTLINE DRAWINGS**".

4.2 ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit	Remarks
Power supply voltage	LCD panel signal processing board	VDD	-0.3 to +14.0	V	Ta = 25°C
	Lamp voltage	VBLH	2,000	Vrms	
Input signal voltage Note1		Vi	-0.3 to +2.8	V	Ta = 25°C VDD=12.0V
Storage temperature		Tst	-20 to +60	°C	-
Operating temperature	Front surface	TopF	0 to +55	°C	Note2
	Rear surface	TopR	0 to + (60)	°C	Note3
Relative humidity Note4		RH	≤ 95	%	Ta ≤ 40°C
			≤ 85	%	40 < Ta ≤ 50°C
			≤ 70	%	50 < Ta ≤ 55°C
Absolute humidity Note4		AH	≤ 73 Note5	g/m^3	Ta > 55°C

Note1: DA0+/-, DA1+/-, DA2+/-, DA3+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, CKB+/-, DC0+/-, DC1+/-, DC2+/-, DC3+/-, CKC+/-, DD0+/-, DD1+/-, DD2+/-, DD3+/-, CKD+/-, CS, SCLK, SDAT, BSEL0, BSEL1

Note2: Measured at center of LCD panel surface (including self-heat)

Note3: Measured at center of LCD module's rear shield surface (including self-heat)

Note4: No condensation

Note5: Ta = 55°C, RH = 70%

4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD panel signal processing board

(Ta = 25°C)

Parameter		Symbol	min.	typ.	max.	Unit	Remarks
Supply voltage		VDD	10.8	12.0	13.2	V	-
Supply current		IDD	-	600 Note1	1,100 Note2	mA	at VDD=12.0V
Ripple voltage		VRP	-	-	100	mVp-p	for VDD
Differential input threshold voltage	High	VTH	-	-	+100	mV	at VCM= 1.2V Note3, Note4
	Low	VTL	-100	-	-	mV	
Input voltage swing		VI	0	-	2.4	V	-
Terminating resistance		RT	-	100	-	Ω	-
Control signal input threshold voltage	High	VIH	High must be Open.			V	Note5
	Low	VIL	0	-	0.5	V	
Control signal input current	Low	IIL	-10	-	10	μA	
Serial communication signal input threshold voltage	High	V+	-	1.4	1.9	V	Note6
	Low	V-	0.4	0.7	-	V	
	Hysteresis	VH	0.3	-	-	V	

Note1: Checkered flag pattern (by EIAJ ED-2522)
Note2: Pattern for maximum current
Note3: Common mode voltage for LVDS driver
Note4: DA0+/-, DA1+/-, DA2+/-, DA3+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, CKB+/-, DC0+/-, DC1+/-, DC2+/-, DC3+/-, CKC+/-, DD0+/-, DD1+/-, DD2+/-, DD3+/-, CKD+/-
Note5: BSEL0, BSEL1
Note6: CS, SCLK, SDAT

4.3.2 Backlight lamp

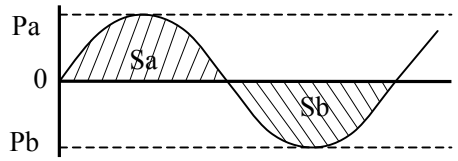
(Ta=25°C, Note1)

Parameter	Symbol	min.	typ.	max.	Unit	Remarks
Lamp current	IBL	3.0	6.0	7.0	mArms	At IBL= 6.0mArms: 800 cd/m^2 Note3
Lamp voltage	VBLH	-	750	-	Vrms	Note2, Note3
Lamp starting voltage	VS	1,220	-	-	Vrms	Ta = 25°C Note2, Note3
		1,460	-	-	Vrms	Ta = 0°C Note2, Note3
Lamp oscillation frequency	FO	50	58	60	kHz	Note4

Note1: This product consists of 6 backlight lamps, and these specifications are for each lamp.

Note2: The lamp voltage cycle between lamps should be kept on a same phase. "VS" and "VBLH" are the voltage value between low voltage side (Cold) and high voltage side (Hot).

Note3: The asymmetric ratio of working waveform for lamps (Lamp voltage peak ratio, Lamp current peak ratio and waveform space ratio) should be less than 5 % (See the following figure.). If the waveform is asymmetric, DC (Direct current) element apply into the lamp. In this case, a lamp lifetime may be shortened, because a distribution of a lamp enclosure substance inclines toward one side between low voltage terminal (Cold terminal) and high voltage terminal (Hot terminal).



$$\frac{|Pa - Pb|}{Pb} \times 100 \leq 5\ \%$$

$$\frac{|Sa - Sb|}{Sb} \times 100 \leq 5\ \%$$

Pa: Supply voltage/current peak for positive, Pb: Supply voltage/current peak for negative
Sa: Waveform space for positive part, Sb: Waveform space for negative part

Note4: In case "FO" is not the recommended value, beat noise may display on the screen, because of interference between "FO" and "1/th". Recommended value of "FO" is as following.

$$FO = \frac{1}{4} \times \frac{1}{th} \times (2n\text{-}1)$$

th: Horizontal cycle period (See "**4.13.1 Timing characteristics**".)
n: Natural number (1, 2, 3 ·····)

Note5: Method of lamp cable installation may invite fluctuation of lamp current and voltage or asymmetric of lamp working waveform. When designing method of lamp cable installation, evaluate the fluctuation of lamp current, voltage and working waveform sufficiently.

4.3.3 Power supply voltage ripple

This product works, even if the ripple voltage levels are beyond the permissible values as following the table, but there might be noise on the display image.

Parameter	Power supply voltage	Ripple voltage Note1 (Measure at input terminal of power supply)	Unit
VDD	12.0 V	≤ 100	mVp-p

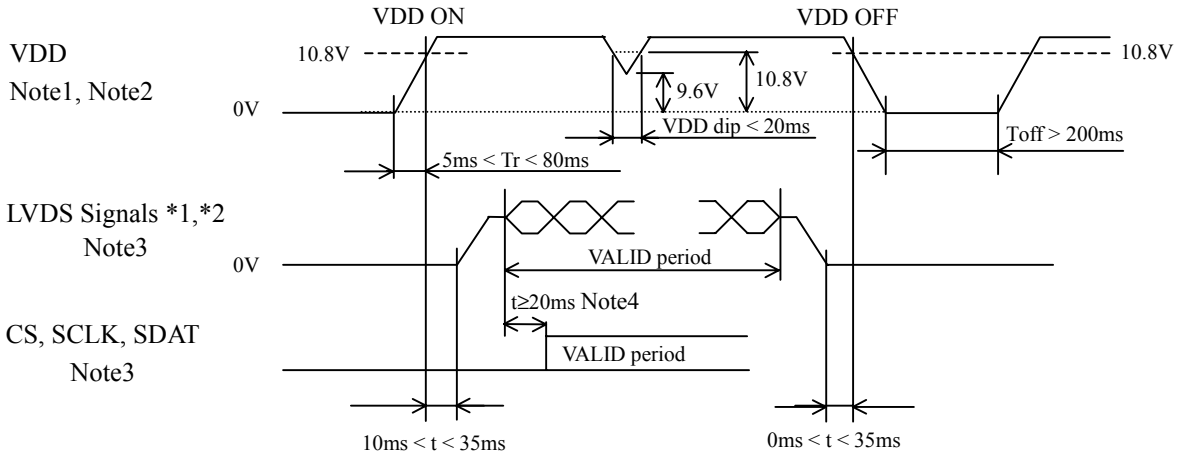
Note1: The permissible ripple voltage includes spike noise.

4.3.4 Fuse

Parameter	Fuse		Rating	Fusing current	Remarks
	Type	Supplier			
VDD	FCC16202AB	KAMYA ELECTRIC Co., Ltd.	2.0 A 32 V	4.0 A	Note1

Note1: The power supply capacity should be more than the fusing current. If the power supply capacity is less than the fusing current, the fuse may not blow for a short time, and then nasty smell, smoking and so on may occur.

4.4 POWER SUPPLY VOLTAGE SEQUENCE



*1: DA0+/-, DA1+/-, DA2+/-, DA3+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, CKB+/-, DC0+/-, DC1+/-, DC2+/-, DC3+/-, CKC+/-, DD0+/-, DD1+/-, DD2+/-, DD3+/-, CKD+/-

*2: LVDS signals should be measured at the terminal of 100Ω resistor.

Note1: In terms of voltage variation (voltage drop) while VDD rising edge is below 10.8V, a protection circuit may work, and then this product may not work.

Note2: VDD should be 10.8V or more during VDD ON period.

Note3: LVDS signals and CS, SCLK, SDAT must be Low or High-impedance, exclude the VALID period (See above sequence diagram), in order to avoid that internal circuits is damaged.
If some of signals are cut while this product is working, even if the signal input to it once again, it might not work normally. If customer stops the display and function signals, they should be cut VDD.

Note4: At the beginning of the serial communication mode, take 20ms or more after the LVDS signal input. When writing the LUT data, see "**4.7 TEN-bit LOOK UP TABLE FOR GAMMA ADJUSTMENT**".

Note5: The backlight inverter voltage should be inputted within the valid period of LVDS signals, in order to avoid unstable data display.

4.5 CONNECTIONS AND FUNCTIONS FOR INTERFACE PINS

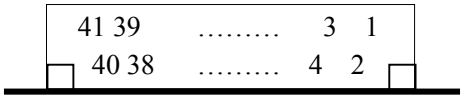
4.5.1 LCD panel signal processing board

CN1 socket (LCD module side): FI-WE41P-HF (Japan Aviation Electronics Industry Limited (JAE))
Adaptable plug: FI-W41S (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Signal	Remarks
1	RSVD1	Reserved	Connect to signal ground.
2	N.C.	-	Keep this pin Open.
3	CS	Chip selection (Pull-up 25kΩ)	LUT communication control signal See "**4.7 TEN-bit LOOK UP TABLE FOP GAMMA ADJUSTMENT**".
4	SCLK	Serial Clock (Pull-down 25kΩ)	
5	SDAT	Serial Data (Pull-down 25kΩ)	
6	RSVD2	Reserved	Keep this pin Open.
7			
8	BSEL0	Selection of LVDS data input map (Pull-up 25kΩ)	See "**4.6 METHOD OF CONNECTION FOR LVDS TRANSMITTER**".
9	BSEL1		
10	RSVD2	Reserved	Keep this pin Open.
11	GND	Signal ground	-
12	DB3+	Pixel data B3	LVDS differential data input Note1
13	DB3-		
14	GND	Signal ground	-
15	CKB+	Pixel clock B	LVDS differential clock input Note1
16	CKB-		
17	GND	Signal ground	-
18	DB2+	Pixel data B2	LVDS differential data input Note1
19	DB2-		
20	GND	Signal ground	-
21	DB1+	Pixel data B1	LVDS differential data input Note1
22	DB1-		
23	GND	Signal ground	-
24	DB0+	Pixel data B0	LVDS differential data input Note1
25	DB0-		
26	GND	Signal ground	-
27	DA3+	Pixel data A3	LVDS differential data input Note1
28	DA3-		
29	GND	Signal ground	-
30	CKA+	Pixel clock A	LVDS differential clock input Note1
31	CKA-		
32	GND	Signal ground	-
33	DA2+	Pixel data A2	LVDS differential data input Note1
34	DA2-		
35	GND	Signal ground	-
36	DA1+	Pixel data A1	LVDS differential data input Note1
37	DA1-		
38	GND	Signal ground	-
39	DA0+	Pixel data A0	LVDS differential data input Note1
40	DA0-		
41	GND	Signal ground	-

Note1: Twist pair wires with 100Ω (Characteristic impedance) should be connected between LCD panel signal processing board and LVDS transmitter.

CN1: View from insert direction

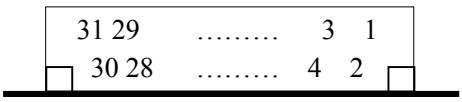


CN2 socket: FI-WE31P-HF (Japan Aviation Electronics Industry Limited (JAE))
Adaptable plug: FI-W31S (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Signal	Remarks
1	GND	Signal ground	-
2	DD3+	Pixel data D3	LVDS differential data input Note1
3	DD3-		
4	GND	Signal ground	-
5	CKD+	Pixel clock D	LVDS differential clock input Note1
6	CKD-		
7	GND	Signal ground	-
8	DD2+	Pixel data D2	LVDS differential data input Note1
9	DD2-		
10	GND	Signal ground	-
11	DD1+	Pixel data D1	LVDS differential data input Note1
12	DD1-		
13	GND	Signal ground	-
14	DD0+	Pixel data D0	LVDS differential data input Note1
15	DD0-		
16	GND	Signal ground	-
17	DC3+	Pixel data C3	LVDS differential data input Note1
18	DC3-		
19	GND	Signal ground	-
20	CKC+	Pixel clock C	LVDS differential clock input Note1
21	CKC-		
22	GND	Signal ground	-
23	DC2+	Pixel data C2	LVDS differential data input Note1
24	DC2-		
25	GND	Signal ground	-
26	DC1+	Pixel data C1	LVDS differential data input Note1
27	DC1-		
28	GND	Signal ground	-
29	DC0+	Pixel data C0	LVDS differential data input Note1
30	DC0-		
31	GND	Signal ground	-

Note1: Twist pair wires with 100Ω (Characteristic impedance) should be connected between LCD panel signal processing board and LVDS transmitter.

CN2: View from insert direction



CN3 socket (LCD module side): IL-Z-8PL-SMTY (Japan Aviation Electronics Industry Limited (JAE))
Adaptable plug: IL-Z-8S-S125C (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Function	Description
1	VDD	Power supply	-
2	VDD		
3	VDD		
4	VDD		
5	GND	Signal ground	-
6	GND		
7	GND		
8	GND		

4.5.2 Backlight lamp

Attention: VBLH and VBLC must be connected correctly. If customer connects wrongly, customer will be hurt and the module will be broken.

CN201 plug (LCD module side): BHSR-02VS-1 (J.S.T. Mfg Co., Ltd.)
Adaptable socket: SM02B-BHSS-1-TB (J.S.T. Mfg Co., Ltd.)

Pin No.	Symbol	Function	Remarks
1	VBLH1	Upper side lamp, High voltage (Hot)	Cable color: (Pink)
2	VBLC1	Upper side lamp, Low voltage (Cold)	Cable color: (White)

CN202 plug (LCD module side): BHSR-02VS-1 (J.S.T. Mfg Co., Ltd.)
Adaptable socket: SM02B-BHSS-1-TB (J.S.T. Mfg Co., Ltd.)

Pin No.	Symbol	Function	Remarks
1	VBLH2	Upper side lamp, High voltage (Hot)	Cable color: (White)
2	VBLC2	Upper side lamp, Low voltage (Cold)	Cable color: (White)

CN203 plug (LCD module side): BHSR-02VS-1 (J.S.T. Mfg Co., Ltd.)
Adaptable socket: SM02B-BHSS-1-TB (J.S.T. Mfg Co., Ltd.)

Pin No.	Symbol	Function	Remarks
1	VBLH3	Upper side lamp, High voltage (Hot)	Cable color: (Blue)
2	VBLC3	Upper side lamp, Low voltage (Cold)	Cable color: (White)

CN204 plug (LCD module side): BHSR-02VS-1 (J.S.T. Mfg Co., Ltd.)
Adaptable socket: SM02B-BHSS-1-TB (J.S.T. Mfg Co., Ltd.)

Pin No.	Symbol	Function	Remarks
1	VBLH4	Lower side lamp, High voltage (Hot)	Cable color: (Pink)
2	VBLC4	Lower side lamp, Low voltage (Cold)	Cable color: (White)

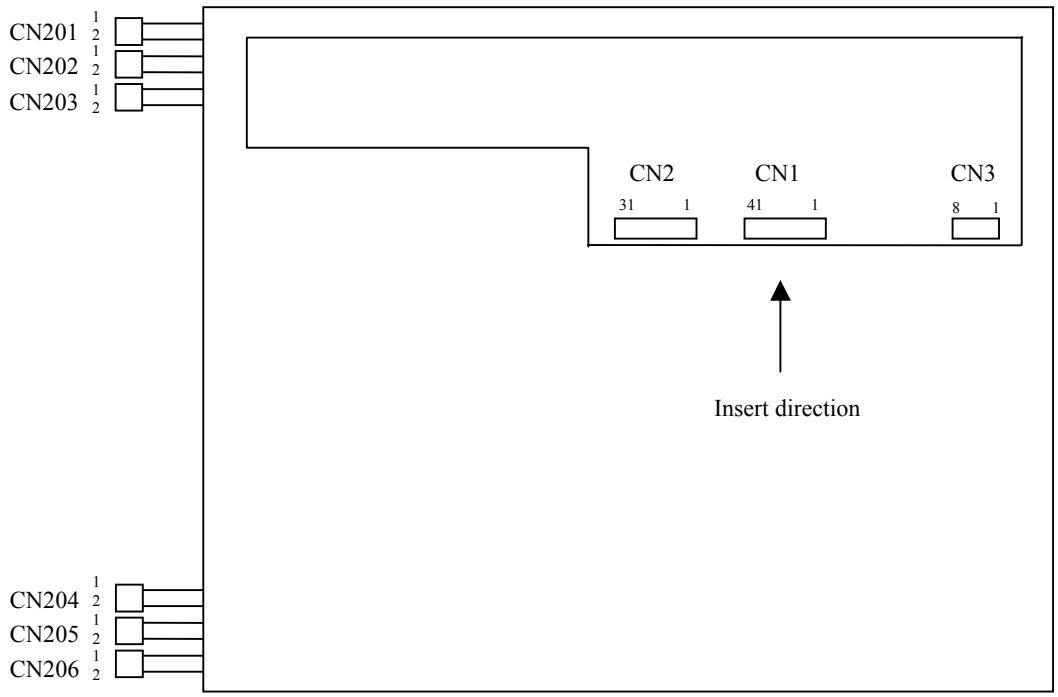
CN205 plug (LCD module side): BHSR-02VS-1 (J.S.T. Mfg Co., Ltd.)
Adaptable socket: SM02B-BHSS-1-TB (J.S.T. Mfg Co., Ltd.)

Pin No.	Symbol	Function	Remarks
1	VBLH5	Lower side lamp, High voltage (Hot)	Cable color: (White)
2	VBLC5	Lower side lamp, Low voltage (Cold)	Cable color: (White)

CN206 plug (LCD module side): BHSR-02VS-1 (J.S.T. Mfg Co., Ltd.)
Adaptable socket: SM02B-BHSS-1-TB (J.S.T. Mfg Co., Ltd.)

Pin No.	Symbol	Function	Remarks
1	VBLH6	Lower side lamp, High voltage (Hot)	Cable color: (Blue)
2	VBLC6	Lower side lamp, Low voltage (Cold)	Cable color: (White)

4.5.3 Positions of plugs and sockets



4.6 METHOD OF CONNECTION FOR LVDS TRANSMITTER

LVDS data input map is selectable with BSEL0 and BSEL1 terminal.

	Bit mapping			Transmitter Pin Assignment					CN1	
	BSEL[1:0] Note1, Note2			Singl type LVDS Tx	Dual type LVDS TX		Output Connector		Pin No.	Signal name
	[H:H], [L:L]	[H:L]	[L:H]		THine THC63LVD823	NS DS90C387				
Pixel data A	LA2	LA7	LA0	TA0	R12	R10				
	LA3	LA6	LA1	TA1	R13	R11		Note3		
	LA4	LA5	LA2	TA2	R14	R12	ATA-	→	40	DA0-
	LA5	LA4	LA3	TA3	R15	R13	ATA+	→	39	DA0+
	LA6	LA3	LA4	TA4	R16	R14				
	LA7	LA2	LA5	TA5	R17	R15				
	CA2	CA7	CA0	TA6	G12	G10				
	CA3	CA6	CA1	TB0	G13	G11				
	CA4	CA5	CA2	TB1	G14	G12				
	CA5	CA4	CA3	TB2	G15	G13	ATB-	→	37	DA1-
	CA6	CA3	CA4	TB3	G16	G14	ATB+	→	36	DA1+
	CA7	CA2	CA5	TB4	G17	G15				
	RA2	RA7	RA0	TB5	B12	B10				
	RA3	RA6	RA1	TB6	B13	B11				
	RA4	RA5	RA2	TC0	B14	B12				
	RA5	RA4	RA3	TC1	B15	B13				
	RA6	RA3	RA4	TC2	B16	B14	ATC-	→	34	DA2-
	RA7	RA2	RA5	TC3	B17	B15	ATC+	→	33	DA2+
	Hsync	Hsync	Hsync	TC4	HSYNC	HSYNC				
	Vsync	Vsync	Vsync	TC5	VSYNC	VSYNC				
	DE	DE	DE	TC6	DE	DE				
	LA0	LA1	LA6	TD0	R10	R16				
	LA1	LA0	LA7	TD1	R11	R17				
	CA0	CA1	CA6	TD2	G10	G16	ATD-	→	28	DA3-
	CA1	CA0	CA7	TD3	G11	G17	ATD+	→	27	DA3+
	RA0	RA1	RA6	TD4	B10	B16				
	RA1	RA0	RA7	TD5	B11	B17				
	N.C.	N.C.	N.C.	TD6	-	-				
	CLK	CLK	CLK	CLK	CLK	CLK	ATCLK-	→	31	CKA-
							ATCLK+	→	30	CKA+
Pixel data B	LB2	LB7	LB0	TA0	R22	R20				
	LB3	LB6	LB1	TA1	R23	R21				
	LB4	LB5	LB2	TA2	R24	R22	BTA-	→	25	DB0-
	LB5	LB4	LB3	TA3	R25	R23	BTA+	→	24	DB0+
	LB6	LB3	LB4	TA4	R26	R24				
	LB7	LB2	LB5	TA5	R27	R25				
	CB2	CB7	CB0	TA6	G22	G20				
	CB3	CB6	CB1	TB0	G23	G21				
	CB4	CB5	CB2	TB1	G24	G22				
	CB5	CB4	CB3	TB2	G25	G23	BTB-	→	22	DB1-
	CB6	CB3	CB4	TB3	G26	G24	BTB+	→	21	DB1+
	CB7	CB2	CB5	TB4	G27	G25				
	RB2	RB7	RB0	TB5	B22	B20				
	RB3	RB6	RB1	TB6	B23	B21				
	RB4	RB5	RB2	TC0	B24	B22				
	RB5	RB4	RB3	TC1	B25	B23				
	RB6	RB3	RB4	TC2	B26	B24	BTC-	→	19	DB2-
	RB7	RB2	RB5	TC3	B27	B25	BTC+	→	18	DB2+
	Hsync	Hsync	Hsync	TC4	HSYNC	HSYNC				
	Vsync	Vsync	Vsync	TC5	VSYNC	VSYNC				
	DE	DE	DE	TC6	DE	DE				
	LB0	LB1	LB6	TD0	R20	R26				
	LB1	LB0	LB7	TD1	R21	R27				
	CB0	CB1	CB6	TD2	G20	G26	BTD-	→	13	DB3-
	CB1	CB0	CB7	TD3	G21	G27	BTD+	→	12	DB3+
	RB0	RB1	RB6	TD4	B20	B26				
	RB1	RB0	RB7	TD5	B21	B27				
	N.C.	N.C.	N.C.	TD6	-	-				
	CLK	CLK	CLK	CLK	CLK	CLK	BTCLK-	→	16	CKB-
							BTCLK+	→	15	CKB+

	BSEL[1:0] Note1, Note2			Singl type LVDS Tx	Dual type LVDS TX		Output Connector		CN2	
	[H:H], [L:L]	[H:L]	[L:H]		THine THC63LVD823	NS DS90C387			Pin No.	Signal name
Pixel data C	LC2	LC7	LC0	TA0	R12	R10				
	LC3	LC6	LC1	TA1	R13	R11		Note3		
	LC4	LC5	LC2	TA2	R14	R12	CTA-	→	30	DC0-
	LC5	LC4	LC3	TA3	R15	R13	CTA+	→	29	DC0+
	LC6	LC3	LC4	TA4	R16	R14				
	LC7	LC2	LC5	TA5	R17	R15				
	CC2	CC7	CC0	TA6	G12	G10				
	CC3	CC6	CC1	TB0	G13	G11				
	CC4	CC5	CC2	TB1	G14	G12				
	CC5	CC4	CC3	TB2	G15	G13	CTB-	→	27	DC1-
	CC6	CC3	CC4	TB3	G16	G14	CTB+	→	26	DC1+
	CC7	CC2	CC5	TB4	G17	G15				
	RC2	RC7	RC0	TB5	B12	B10				
	RC3	RC6	RC1	TB6	B13	B11				
	RC4	RC5	RC2	TC0	B14	B12				
	RC5	RC4	RC3	TC1	B15	B13				
	RC6	RC3	RC4	TC2	B16	B14	CTC-	→	24	DC2-
	RC7	RC2	RC5	TC3	B17	B15	CTC+	→	23	DC2+
	Hsync	Hsync	Hsync	TC4	HSYNC	HSYNC				
	Vsync	Vsync	Vsync	TC5	VSYNC	VSYNC				
	DE	DE	DE	TC6	DE	DE				
	LC0	LC1	LC6	TD0	R10	R16				
	LC1	LC0	LC7	TD1	R11	R17				
	CC0	CC1	CC6	TD2	G10	G16	CTD-	→	18	DC3-
	CC1	CC0	CC7	TD3	G11	G17	CTD+	→	17	DC3+
	RC0	RC1	RC6	TD4	B10	B16				
	RC1	RC0	RC7	TD5	B11	B17				
	N.C.	N.C.	N.C.	TD6	-	-				
	CLK	CLK	CLK	CLK	CLK	CLK	CTCLK-	→	21	CKC-
							CTCLK+	→	20	CKC+
Pixel data D	LD2	LD7	LD0	TA0	R22	R20				
	LD3	LD6	LD1	TA1	R23	R21				
	LD4	LD5	LD2	TA2	R24	R22	DTA-	→	15	DD0-
	LD5	LD4	LD3	TA3	R25	R23	DTA+	→	14	DD0+
	LD6	LD3	LD4	TA4	R26	R24				
	LD7	LD2	LD5	TA5	R27	R25				
	CD2	CD7	CD0	TA6	G22	G20				
	CD3	CD6	CD1	TB0	G23	G21				
	CD4	CD5	CD2	TB1	G24	G22				
	CD5	CD4	CD3	TB2	G25	G23	DTB-	→	12	DD1-
	CD6	CD3	CD4	TB3	G26	G24	DTB+	→	11	DD1+
	CD7	CD2	CD5	TB4	G27	G25				
	RD2	RD7	RD0	TB5	B22	B20				
	RD3	RD6	RD1	TB6	B23	B21				
	RD4	RD5	RD2	TC0	B24	B22				
	RD5	RD4	RD3	TC1	B25	B23				
	RD6	RD3	RD4	TC2	B26	B24	DTC-	→	9	DD2-
	RD7	RD2	RD5	TC3	B27	B25	DTC+	→	8	DD2+
	Hsync	Hsync	Hsync	TC4	HSYNC	HSYNC				
	Vsync	Vsync	Vsync	TC5	VSYNC	VSYNC				
	DE	DE	DE	TC6	DE	DE				
	LD0	LD1	LD6	TD0	R20	R26				
	LD1	LD0	LD7	TD1	R21	R27				
	CD0	CD1	CD6	TD2	G20	G26	DTD-	→	3	DD3-
	CD1	CD0	CD7	TD3	G21	G27	DTD+	→	2	DD3+
	RD0	RD1	RD6	TD4	B20	B26				
	RD1	RD0	RD7	TD5	B21	B27				
	N.C.	N.C.	N.C.	TD6	-	-				
	CLK	CLK	CLK	CLK	CLK	CLK	DTCLK-	→	6	CKD-
							DTCLK+	→	5	CKD+

Note1: High must be Open.

Note2: Do not change the setting of BSEL0 and BSEL1 during VDD ON period.

Note3: Twist pair wires with 100Ω (Characteristic impedance) should be connected between LCD panel signal processing board and LVDS transmitter.

4.7 TEN-bit LOOK UP TABLE FOR GAMMA ADJUSTMENT

Adjustment of gamma characteristics for each 8-bit LCR data is possible by using built-in 10-bit LUT (look up table) for Gamma characteristics.

The LUT is set with the serial data. The combination of the control command determines Random/Sequential Address WRITE and Individual/Simultaneous LCR setting.

The serial data is composed as Table1.

Table1: Serial data Composition

DATA	DATA name	Function	Remarks
D31	CMD5	Control Command	See Table2 and Table3.
D30	CMD4	Control Command	
D29	CMD3	Control Command	
D28	CMD2	Control Command	
D27	CMD1	Control Command	
D26	CMD0	Control Command	
D25	ADD9	LUT Address (MSB)	See Table4.
D24	ADD8	LUT Address	
D23	ADD7	LUT Address	
D22	ADD6	LUT Address	
D21	ADD5	LUT Address	
D20	ADD4	LUT Address	
D19	ADD3	LUT Address	
D18	ADD2	LUT Address	
D17	ADD1	LUT Address	
D16	ADD0	LUT Address (LSB)	
D15	DATA15	LUT Data (MSB)	See Table5.
D14	DATA14	LUT Data	
D13	DATA13	LUT Data	
D12	DATA12	LUT Data	
D11	DATA11	LUT Data	
D10	DATA10	LUT Data	
D9	DATA9	LUT Data	
D8	DATA8	LUT Data	
D7	DATA7	LUT Data	
D6	DATA6	LUT Data	
D5	DATA5	LUT Data	
D4	DATA4	LUT Data	
D3	DATA3	LUT Data	
D2	DATA2	LUT Data	
D1	DATA1	LUT Data	
D0	DATA0	LUT Data (LSB)	

Table2: Command table (CMD5 to CMD0: 6-bit)

DATA name	Parameter	Remarks
CMD5	Must be set to "1".	-
CMD4	Must be set to "1".	-
CMD3	Selection of Random/Sequential Address WRITE "1": Random Address WRITE "0": Sequential Address WRITE	-
CMD2	Must be set to "1".	-
CMD1	Selection of Individual/Simultaneous LCR setting "1": Individual LCR setting "0": Simultaneous LCR setting	"1": Select the Dot by using ADD9 and ADD8. (See Table4.) "0": ADD9 and ADD8 are invalid.
CMD0	Must be set to "0".	-

Table3: Command table (CMD5 to CMD0: 6-bit)

CMD5	CMD4	CMD3	CMD2	CMD1	CMD0	Function
1	1	1	1	1	0	Random Address WRITE, Individual LCR setting
1	1	1	1	0	0	Random Address WRITE, Simultaneous LCR setting
1	1	0	1	1	0	Sequential Address WRITE, Individual LCR setting
1	1	0	1	0	0	Sequential Address WRITE, Simultaneous LCR setting

*Another combinations are prohibited, and may cause function error.

Table4: Address table (ADD9 to ADD0: 10-bit)

DATA name	Parameter	Remarks
ADD9 ADD8	Dot Selection ADD[9:8]= 0:0 Left Dot 0:1 Center Dot 1:0 Right Dot 1:1 ON/OFF selection of Gamma Correction	In case of "ADD[9:8]=1:1", ON/OFF of Gamma correction can select according to the GMA[2:0]. (See Table6 and Table7.)
ADD7 ADD6 ADD5 ADD4 ADD3 ADD2 ADD1 ADD0	LUT Address 256 address = 00h - FFh	If "ADD[9:8] = 1:1", ADD[7:0] must be set to 00h.

Table5: Data table (DATA15 to DATA0: 16bit)

DATA	DATA name	Parameter	Remarks
DATA15	Dummy	Dummy Data Must be set to "0".	-
DATA14	Dummy		
DATA13	Dummy		
DATA12	Dummy		
DATA11	Dummy		
DATA10	Dummy		
DATA9	DATA9	[MSB]	-
DATA8	DATA8		
DATA7	DATA7		
DATA6	DATA6		
DATA5	DATA5	10-bit LUT Data 000h - 3FFh	
DATA4	DATA4		
DATA3	DATA3		
DATA2	DATA2		
DATA1	DATA1		
DATA0	DATA0	[LSB]	

Table6: Gamma correction table (DATA15 to DATA0: 16bit)

DATA	DATA name	Parameter	Remarks
DATA15	Dummy	Dummy Data Must be set to "0".	-
DATA14	Dummy		
DATA13	Dummy		
DATA12	Dummy		
DATA11	Dummy		
DATA10	Dummy		
DATA9	Dummy		
DATA8	Dummy		
DATA7	Dummy		
DATA6	Dummy		
DATA5	Dummy		
DATA4	Dummy		
DATA3	Dummy		
DATA2	GAM2	[MSB]	See Table7.
DATA1	GAM1	GMA Data	
DATA0	GAM0	[LSB]	

Table7: Control code GAM[2:0]

GMA2	GMA1	GMA0	Function
0	0	0	No correction (Initial setting)
0	0	1	Correction according to the LUT Data.

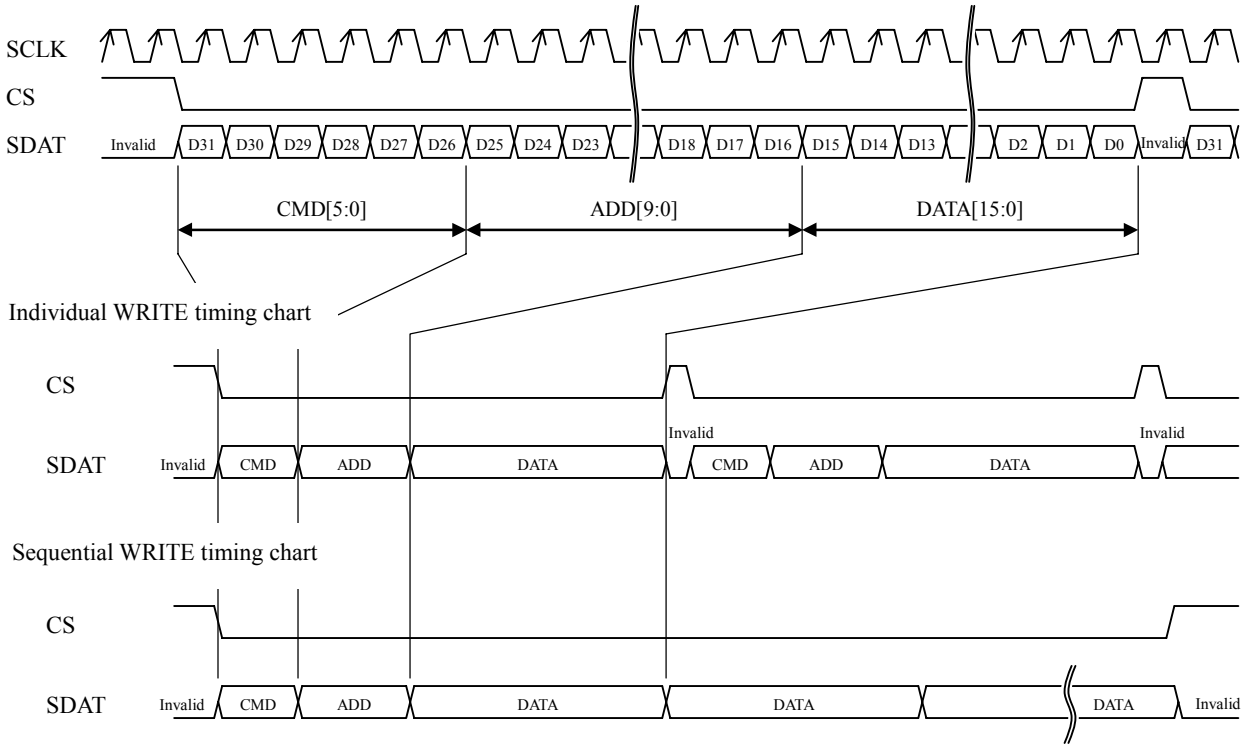
*Another combinations are prohibited, and may cause function error.

Note1: When writing the LUT data, a noise may appear on the display image. In order to prevent the noise appearing on the display, following measures should be performed.
(1) The LUT data should be rewritten during invalid period of pixel data (See "**4.13 INPUT SIGNAL TIMINGS**".).
(2) The LUT data should be rewritten while the LUT data is invalid.

Note2: Because the LUT data isn't stored in the LCD module, transfer the data every power-on.

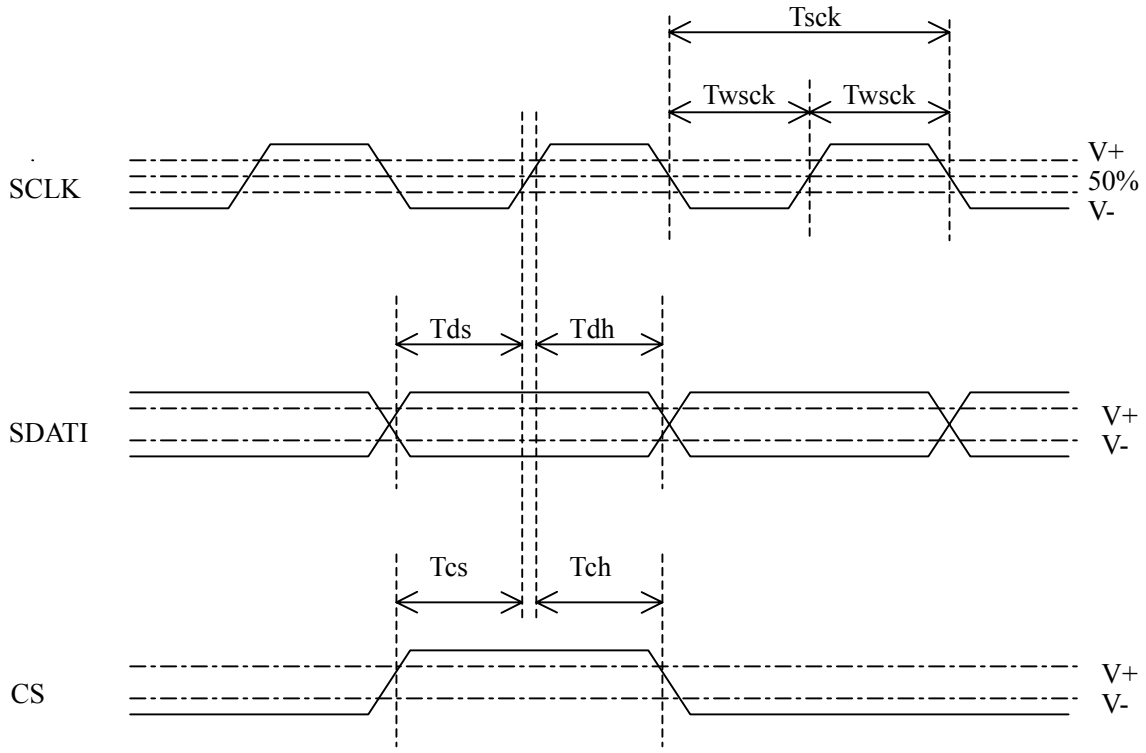
4.8 LUT SERIAL COMMUCATION TIMINGS

(1) Timing chart



(3) Timing specifications

Parameter	Symbol	min.	typ.	max.	Unit
SCLK Frequency	1/Tsck	-	-	5	MHz
SCLK Pulse	Twsck	50	-	-	ns
SDAT-SCLK Setup Time	Tds	50	-	-	ns
SDAT-SCLK Hold Time	Tdh	50	-	-	ns
CS-SCLK Setup Time	Tcs	50	-	-	ns
CS-SCLK Hold Time	Tch	50	-	-	ns



Note1: During the serial communication mode, the display noise may appear because of rewriting the data. To avoid this, rewrite the data in the blanking timing. The external noise may cause the data change, refresh the data regularly according to need.

4.9 DISPLAY GRAY SCALE AND INPUT DATA SIGNALS

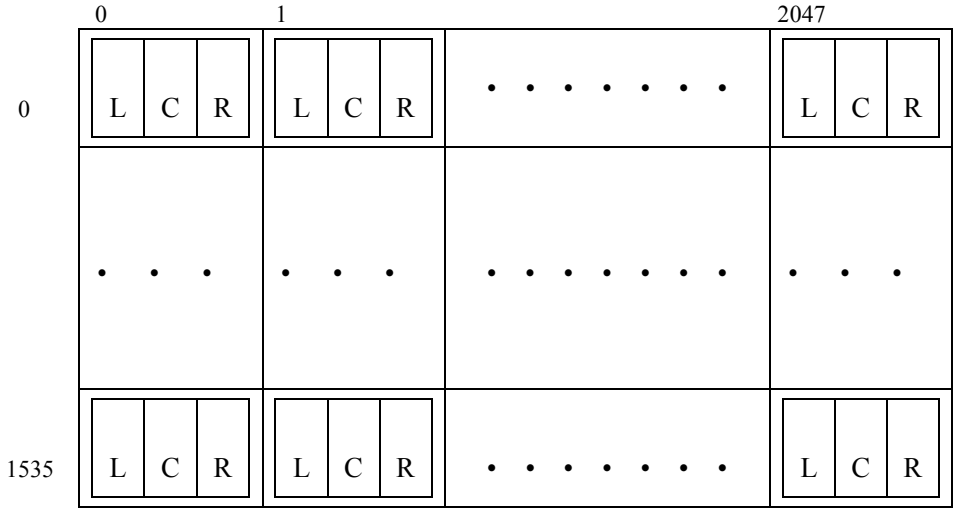
This product can display 256 gray scale in each LCR Dot and 766 gray scale per 1 pixel. Also the relation between display gray scale and input data signals is as the following table.

Display gray scale		Data signal (0: Low level, 1: High level)																									
		LA7	LA6	LA5	LA4	LA3	LA2	LA1	LA0	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0
		LB7	LB6	LB5	LB4	LB3	LB2	LB1	LB0	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
		LC7	LC6	LC5	LC4	LC3	LC2	LC1	LC0	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0
		LD7	LD6	LD5	LD4	LD3	LD2	LD1	LD0	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0
Left-dot Gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	↑	:								:								:							
	↓	:								:								:							
	bright	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Center-dot Gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	↑	:								:								:							
	↓	:								:								:							
	bright	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	White	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Right-dot Gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	↑	:								:								:							
	↓	:								:								:							
	bright	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	White	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

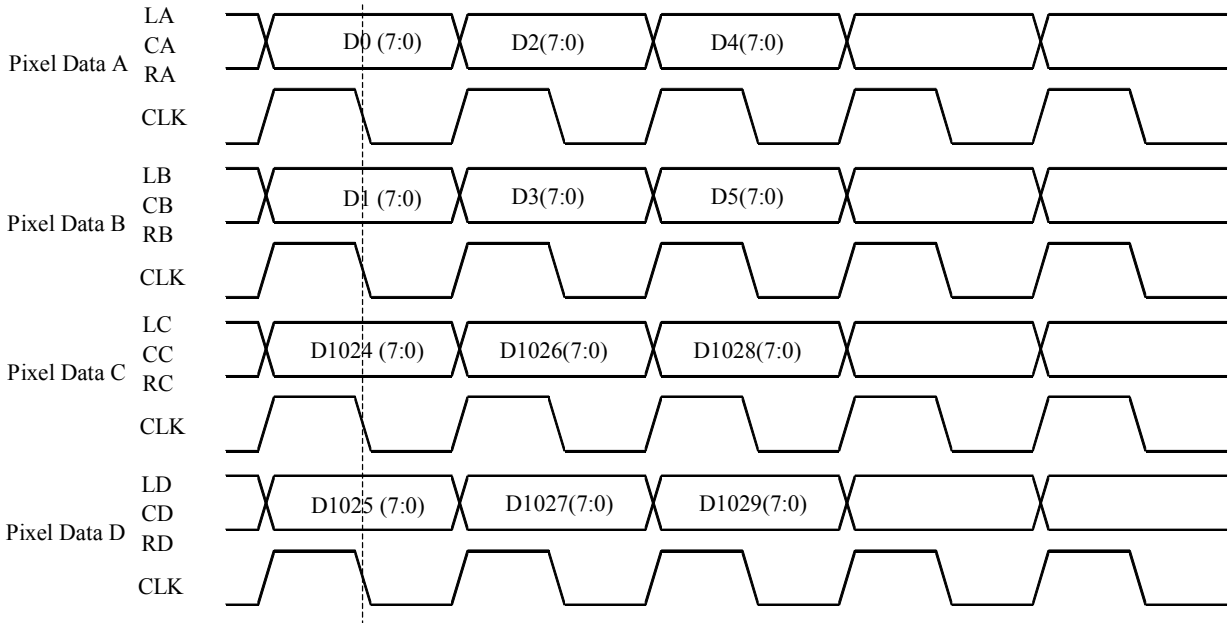
4.10 DISPLAY POSITIONS

0, 0	1,0	• • •	1022, 0	1023, 0	1024, 0	1025, 0	• • •	2046, 0	2047, 0
0, 1	1,1	• • •	1022, 1	1023, 1	1024, 1	1025, 1	• • •	2046, 1	2047, 1
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
0, 1534	1, 1534	• • •	1022, 1534	1023, 1534	1024, 1534	1025, 1534	• • •	2046, 1534	2047, 1534
0, 1535	1, 1535	• • •	1022, 1535	1023, 1535	1024, 1535	1025, 1535	• • •	2046, 1535	2047, 1535

4.11 PIXEL ARRANGNMENT



4.12 LVDS DATA TARANSMISSION METHOD



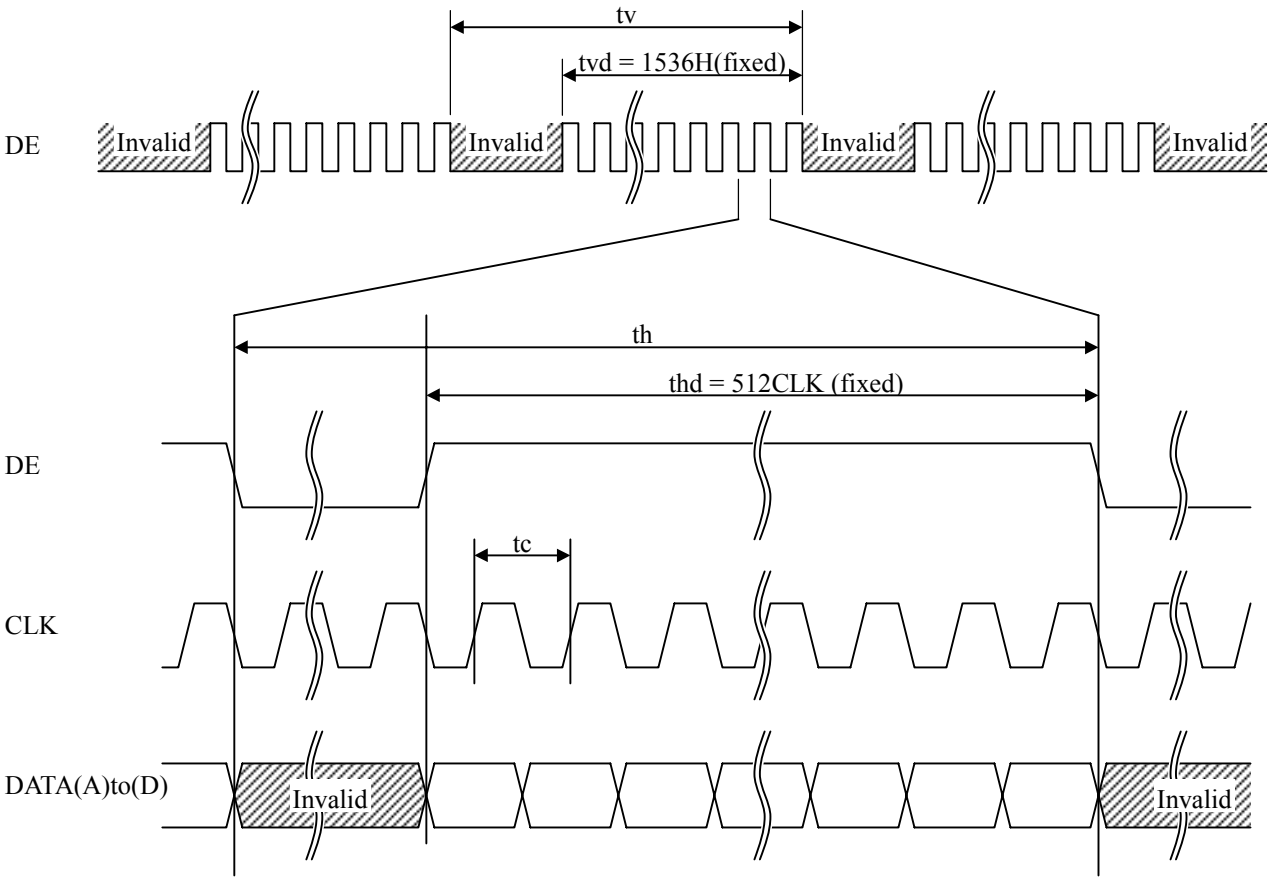
4.13 INPUT SIGNAL TIMINGS

4.13.1 Timing characteristics

Parameter		Symbol	min.	typ.	max.	Unit	Remarks	
CLK	Frequency	1/ tc	60.0	65.0	66.0	MHz	-	
		tc	-	15.38	-	ns		
	Duty	-	See the data sheet of LVDS transmitter.			-	-	
	Rise, fall	-				ns	-	
DE	Horizontal Period	th	10.00 640	10.339 672	10.77 700	µs CLK	typ.=96.72kHz Note1, Note2	6
	Horizontal Display period	thd	512			CLK	-	
	Vertical Period	tv	15.47 1,547	16.667 1,612	17.9 1,628	ms H	typ.=60.0Hz	6
	Vertical Display period	tvd	1,536			H	-	
	CLK-DE set-up	-	See the data sheet of LVDS transmitter.			ns	-	
	CLK-DE hold	-				ns	-	
	Raise,fall	-				ns	-	
DATA (A) to (D)	CLK-DATA set-up	-	See the data sheet of LVDS transmitter.			ns	-	
	CLK-DATA hold	-				ns	-	
	Rise, fall	-				ns	-	

Note1: Both of "time" and "CLK number" of the "th" must keep the Minimum value of specification.
Note2: The sum of jitter and skew of horizontal period should be within ±1 CLK.

4.13.2 Input signals timing chart



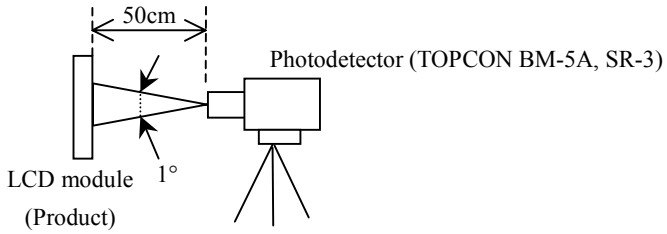
4.14 OPTICS

4.14.1 Optical characteristics

(Note1, Note2)

Parameter		Condition	Symbol	min.	typ.	max.	Unit	Measuring instrument	Remarks	
Luminance		White at center θR = 0°, θL = 0°, θU = 0°, θD = 0°	L	700	800	-	cd/m^2	SR-3	-	6
Contrast ratio		White/Black at center θR = 0°, θL = 0°, θU = 0°, θD = 0°	CR	450	700	-	-	SR-3	Note3	6
Luminance uniformity		-	LU	-	1.2	1.3	-	BM-5A	Note4	6
Chromaticity	White	**x** coordinate	Wx	-	0.255	-	-	SR-3	Note5	
		y coordinate	Wy	-	0.310	-	-			
Response time		Black to White	Ton	-	(17)	25	ms	BM-5A	Note6 Note7	6
		White to Black	Toff	-	(18)	25	ms			
Viewing angle	Right	θU = 0°, θD = 0°, CR ≥ 10	θR	70	85	-	°	BM-5A	Note8	
	Left	θU = 0°, θD = 0°, CR ≥ 10	θL	70	85	-	°			
	Up	θR = 0°, θL = 0°, CR ≥ 10	θU	70	85	-	°			
	Down	θR = 0°, θL = 0°, CR ≥ 10	θD	70	85	-	°			

Note1: These are initial characteristics.
Note2: Measurement conditions are as follows.
Ta = 25°C, VDD = 12.0V, IBL = 6.0mArms/lamp, Display mode: QXGA,
Horizontal cycle = 95.34kHz, Vertical cycle = 60.0Hz
Optical characteristics are measured after 20 minutes from working the product, in the dark room. Also measurement method for luminance is as follows.



Note3: See "**4.14.2 Definition of contrast ratio**".
Note4: See "**4.14.3 Definition of luminance uniformity**".
Note5: These coordinates are found on CIE 1931 chromaticity diagram.
Note6: Product surface temperature: TopF = 35°C 6
Note7: See "**4.14.4 Definition of response times**".
Note8: See "**4.14.5 Definition of viewing angles**".

4.14.2 Definition of contrast ratio

The contrast ratio is calculated by using the following formula.

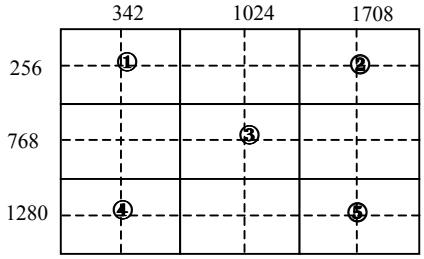
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance of white screen}}{\text{Luminance of black screen}}$$

4.14.3 Definition of luminance uniformity

The luminance uniformity is calculated by using following formula.

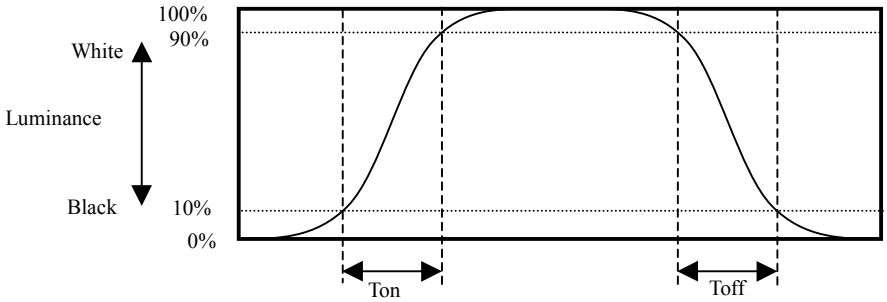
$$\text{Luminance uniformity (LU)} = \frac{\text{Maximum luminance from ① to ⑤}}{\text{Minimum luminance from ① to ⑤}}$$

The luminance is measured at the 9 points shown below.

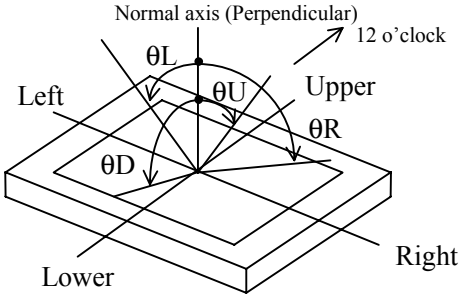


4.14.4 Definition of response times

Response time is measured, the luminance changes from "black" to "white", or "white" to "black" on the same screen point, by photo-detector. Ton is the time it takes the luminance change from 10% up to 90%. Also Toff is the time it takes the luminance change from 90% down to 10% (See the following diagram.).



4.14.5 Definition of viewing angles

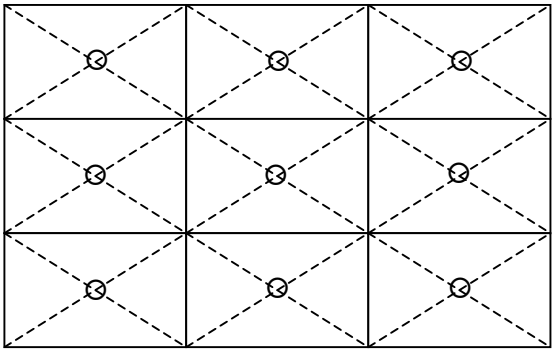


5. RELIABILITY TESTS

Test item		Condition	Judgment Note1
High temperature and humidity (Operation)		① 60 ± 2°C, RH = 60%, 240hours ② Display data is white.	No display malfunctions
Heat cycle (Operation)		① 0 ± 3°C…1hour 55 ± 3°C…1hour ② 50cycles, 4hours/cycle ③ Display data is white.	
Thermal shock (Non operation)		① -20 ± 3°C…30minutes 60 ± 3°C…30minutes ② 100cycles, 1hour/cycle ③ Temperature transition time is within 5 minutes.	
Vibration (Non operation)		① 5 to 100Hz, 11.76m/s^2 ② 1 minute/cycle ③ X, Y, Z direction ④ 10 times each directions	No display malfunctions No physical damages
Mechanical shock (Non operation)		① 294m/ s^2, 11ms ② X, Y, Z direction ③ 3 times each directions	
ESD (Operation)		① 150pF, 150Ω, ±10kV ② 9 places on a panel surface Note2 ③ 10 times each places at 1 sec interval	No display malfunctions
Dust (Operation)		① Sample dust: No.15 (by JIS-Z8901) ② 15 seconds stir ③ 8 times repeat at 1 hour interval	
Low pressure	non-operation	① 15 kPa ② -20°C±3°C…24 hours ③ 60°C±3°C…24 hours	
	operation	① 53.3 kPa ② 0°C±3°C…24 hours ③ 55°C±3°C…24 hours	

Note1: Display and appearance are checked under environmental conditions equivalent to the inspection conditions of defect criteria.

Note2: See the following figure for discharge points



6. PRECAUTIONS

6.1 MEANING OF CAUTION SIGNS

The following caution signs have very important meaning. **Be sure to read "6.2 CAUTIONS" and "6.3 ATTENTIONS", after understanding this contents!**

This sign has the meaning that customer will be injured by himself or the product will sustain a damage, if customer has wrong operations.

This sign has the meaning that customer will get an electrical shock, if customer has wrong operations.

This sign has the meaning that customer will be injured by himself, if customer has wrong operations.

6.2 CAUTIONS

∗ Do not touch the working backlight. Customer will be in danger of an electric shock.

∗ Do not touch the working backlight. Customer will be in danger of burn injury.
∗ Do not shock and press the LCD panel and the backlight! There is a danger of breaking, because they are made of glass. (Shock: To be not greater 294m/s^2 and to be not greater 11ms, Pressure: To be not greater 19.6 N)

6.3 ATTENTIONS

6.3.1 Handling of the product

① Take hold of both ends without touch the circuit board cover when customer pulls out products (LCD modules) from inner packing box. If customer touches it, products may be broken down or out of adjustment, because of stress to mounting parts.
② Do not hook cables nor pull connection cables such as lamp cable and so on, for fear of damage.
③ If customer puts down the product temporarily, the product puts on flat subsoil as a display side turns down.
④ Take the measures of electrostatic discharge such as earth band, ionic shower and so on, when customer deals with the product, because products may be damaged by electrostatic.
⑤ The torque for mounting screws must never exceed 0.735 N·m. Higher torque values might result in distortion of the bezel.
⑥ The product must be installed using mounting holes without undue stress such as bends or twist (See outline drawings). And do not add undue stress to any portion (such as bezel flat area) except mounting hole portion.
Bends or twist described above and undue stress to any portion except mounting hole portion may cause display un-uniformity.

⑦ Do not press or rub on the sensitive display surface. If customer clean on the panel surface, NEC recommends using the cloth with ethanolic liquid such as screen cleaner for LCD.
⑧ Do not push-pull the interface connectors while the product is working, because wrong power sequence may break down the product.

6.3.2 Environment

① Do not operate or store in high temperature, high humidity, dewdrop atmosphere or corrosive gases. Keep the product in antistatic pouch in room temperature, because of avoidance for dusts and sunlight, if customer stores the product.
② In order to prevent dew condensation occurring by temperature difference, the product packing box must be opened after leave under the environment of an unpacking room temperature enough. Because a situation of dew condensation occurring is changed by the environmental temperature and humidity, evaluate the leaving time sufficiently. (Recommendation leaving time: 6 hour or more with packing state)
③ Do not operate in high magnetic field. Circuit boards may be broken down by it.
④ This product is not designed as radiation hardened.
⑤ Use an original protection sheet on the product surface (polarizer). Adhesive type protection sheet should be avoided, because it may change color or properties of the polarizer.

6.3.3 Characteristics

The following items are neither defects nor failures.

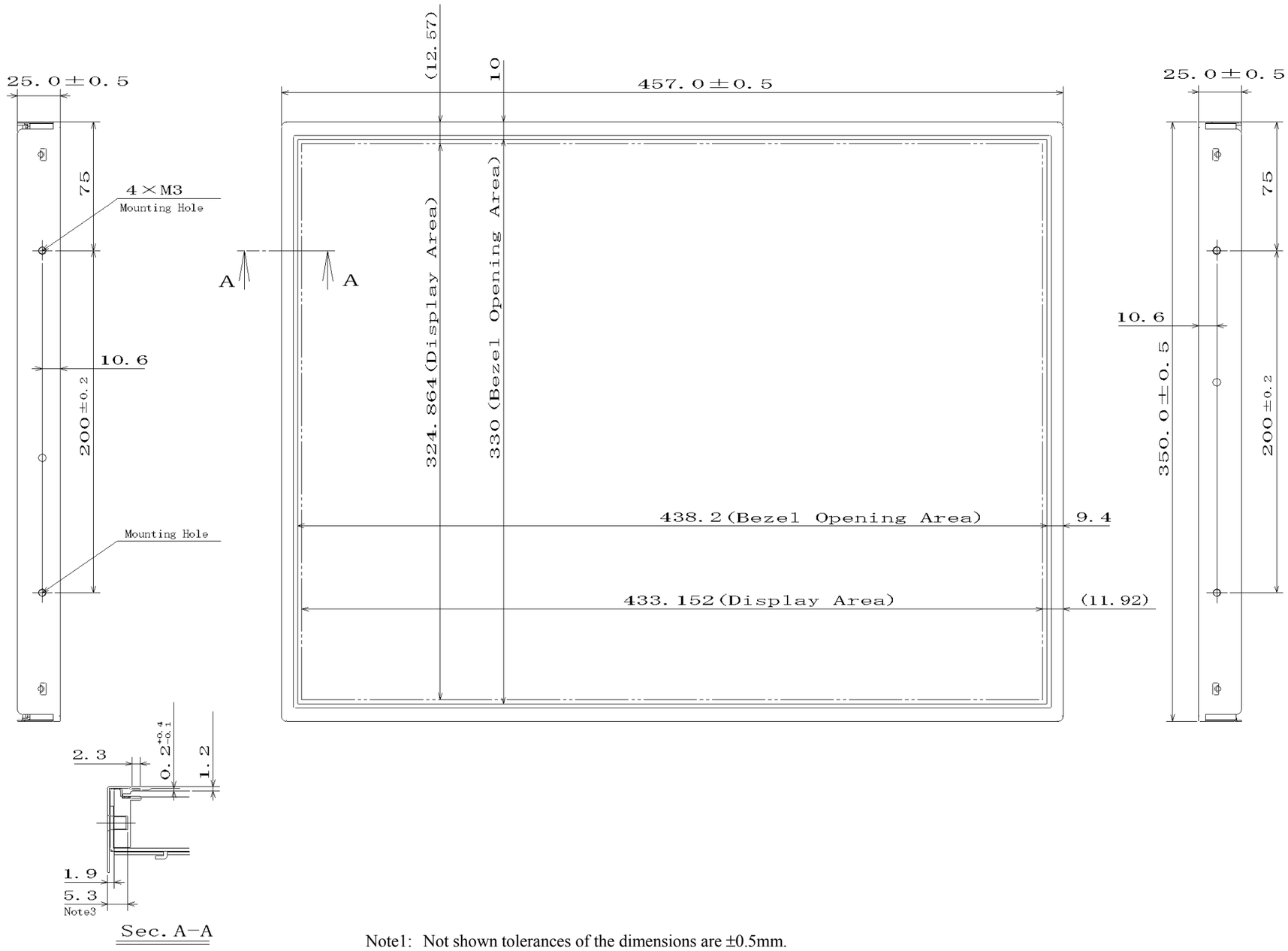
① Response time and luminance may be changed by ambient temperature.
② The LCD may be seemed luminance non-uniformity, flicker, vertical seam or small spot by display patterns.
③ Optical characteristics (e.g. luminance, display uniformity, etc.) gradually is going to change depending on operating time, and especially low temperature, because the LCD has cold cathode fluorescent lamps.
④ Do not display the fixed pattern for a long time because it may cause image sticking. Use a screen saver, if the fixed pattern is displayed on the screen.
⑤ Optical characteristics may be changed by input signal timings.
⑥ The interference noise of input signal frequency for this product's signal processing board and luminance control frequency of customer's backlight inverter may appear on a display. Set up luminance control frequency of backlight inverter so that the interference noise does not appear.

6.3.4 Other

① All GND and VDD terminals should be connected without a non-connected signal line.
② Do not disassemble a product or adjust volume without permission of NEC.
③ Pay attention not to insert waste materials inside of products, if customer uses screwnails.
④ Pack the product with original shipping package, because of avoidance of some damages during transportation, when customer returns it to NEC for repair and so on.
⑤ The LCD module by itself or integrated into end product should be packed and transported with display in the vertically position. Otherwise the display characteristics may be impaired.

7. OUTLINE DRAWINGS

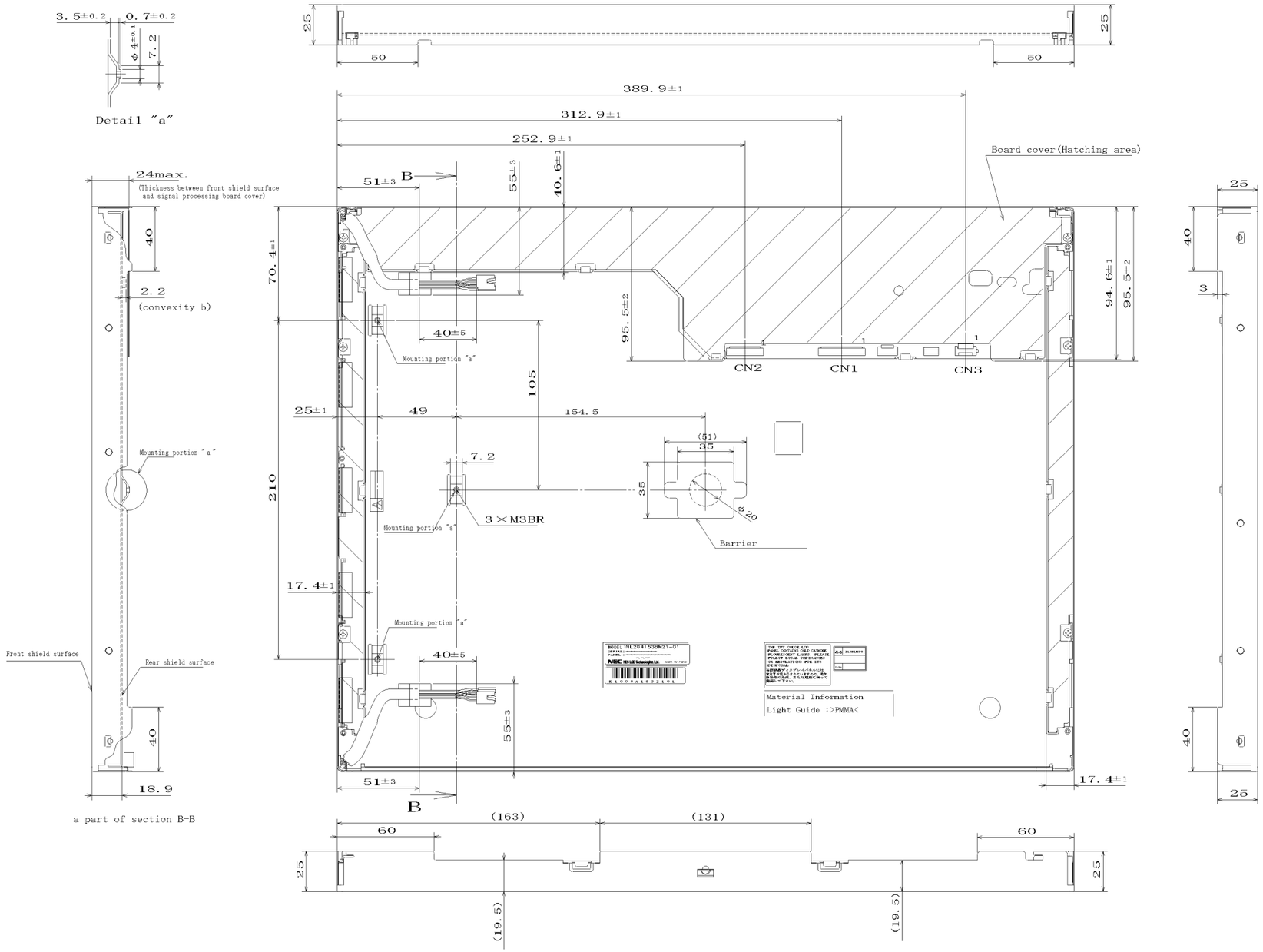
7.1 FRONT VIEW



Note1: Not shown tolerances of the dimensions are ±0.5mm.
Note2: The torque for mounting screws must be 0.735N·m.
Note3: The length of mounting screws from surface of plate must be ≤ 5.3mm.
Note4: The values in parentheses are for reference.

Unit: mm

7.2 REAR VIEW



Note1: Not shown tolerances of the dimensions are ±0.5mm.
Note2: The torque for mounting screws must be 0.735N·m.
Note3: The values in parentheses are for reference.

Unit: mm

REVISION HISTORY

The inside of latest specifications is revised to the clerical error and the major improvement of previous edition. Only a changed part such as functions, characteristic value and so on that may affect a design of customers, are described especially below.

Edition	Document number	Prepared date	Revision contents and signature
1st edition	DOD-MA-0117	Sep. 25, 2002	**Revision contents** New issue **Signature of writer** *Approved by* T. SHIMIZU — *Checked by* ——— — *Prepared by* M. ITO
2nd edition	DOD-M-1248	Nov. 28, 2002	**Revision contents** • With an inverter → Inverter less • Direct type backlight → Edge light type backlight P4 Outline (changed) Features (changed) P5 Outline characteristics (changed) P6 Block diagram (changed) P7 General specifications (changed) Absolute maximum ratings (changed) P8 Electrical characteristics (changed) P11 Power supply voltage sequence (changed) P12 Interface pin connections and functions (changed) P17 Method of connection for THC63LVD823 (correction) P20 Input signal timings (changed) P23 Optical characteristics (changed) P25 Reliability tests (added) P26 Precautions (added) P28 Outline drawings (revised) **Signature of writer** *Approved by* T. ITO — *Checked by* ——— — *Prepared by* R. KAWASHIMA
3rd edition	DOD-PD-0006	April 7, 2003	**Revision contents** P1 Type name: NL204153BC21-xx → NL204153BM21-xx (correction) P5 Module size: 25.0mm max. → 25.0mm typ. (correction) Backlight-Replaceable parts (deleted) Power consumption: (40)W → TBD P6 Block diagram (changed) P7 Absolute maximum ratings: Note1, Note2 (added) P8 Controller / LCD driving: Note1, Note2 (added) P12 Interface pin connections and functions-CN1: Pin No1 to 10 (changed) P14 (4) Data conversion table (added) P15 LVDS data transmission mode (deleted) P15 Method of connection for LVDS transmitter (changed) P17 10-bit look up table (added) P24 Attentions (revised) **Signature of writer** *Approved by* T. ITO — *Checked by* ——— — *Prepared by* R. KAWASHIMA

REVISION HISTORY

Edition	Document number	Prepared date	Revision contents and signature
4th edition	DOD-PD-0096	July 4, 2003	**Revision contents** P1 Type name: → NL204153BM21-01 P9 Driving for backlight lamp- Lamp starting voltage (VS): • Ta= 25°C: (1000) Vrms→ (1220) Vrms • Ta= 0°C: (1300) Vrms→ (1460) Vrms P18 Input signal specifications are changed. P20 "LVDS data transmission method" is added. P23 Reliability tests: Note1 is changed. P26 Outline drawings are changed. **Signature of writer** *Approved by* T. ITO *Checked by* ——— *Prepared by* R. KAWASHIMA
5th edition	DOD-PD-0246	Oct. 27, 2003	**Revision contents** Data correction or implementation depend on the specification review P5: 2.GENERAL SPECIFICATIONS P6: 3.BLOCK DIAGRAM P7: 4.1 MECHANICAL SPECIFICATIONS 4.2 ABSOLUTE MAXIMUM RATINGS P8-P10: 4.3 ELECTRICAL CHARACTERISTICS 4.3.1 LCD panel signal processing board 4.3.2 Backlight lamp 4.3.5 Fuse P11: POWER SUPPLY VOLTAGE SEQUENCE P12-P14: 4.5 CONNECTIONS AND FUNCTIONS FOR INTERFACE PINS 4.5.1 LCD panel signal processing board-CN1 4.5.2 Backlight lamp P16, P17: METHOD OF CONNECTION FOR LVDS TRANSMITTER P24: 4.10 DISPLAY POSITIONS P25: 4.12 LVDS DATA TARANSMISSION METHOD P26: 4.13 INPUT SIGNAL TIMINGS P27: 4.14.1 Optical characteristics P30, P31: 6. Precautions P32, P33: 7. OUTLINE DRAWINGS New paragraph (Addition) P18-P20: 4.7 TEN-bit LOOK UP TABLE FOR GAMMA ADJUSTMENT P21, P22: 4.8 LUT SERIAL COMMUCATION TIMINGS **Signature of writer** *Approved by* T. ITO *Checked by* ——— *Prepared by* R. KAWASHIMA

REVISION HISTORY

Edition	Document number	Prepared date	Revision contents and signature
6th edition	DOD-PD-0418	Mar. 5, 2004	**Revision contents** P5, 27 Contrast ratio: (650):1 typ. → 700:1 typ. P5 GENERAL SPECIFICATIONS • Designed viewing direction: Viewing angle with optimum grayscale (γ=2.2) → Viewing angle with optimum grayscale (γ=DICOM) • Response time: (32) ms typ. → (35) ms typ. P7 ABSOLUTE MAXIMUM RATINGS • Lamp voltage: → 2,000 Vrms P8 LCD panel signal processing board • Supply current: (1,180)mA max. → 1,100mA max. P9 Backlight lamp • Lamp oscillation frequency: → 50kHz min., 60kHz max. P26 INPUT SIGNAL TIMINGS- Timing characteristics • th: → 10.00μs min., 10.77μs max. • tv: → 15.47ms min., 17.9ms max. P27 Optical characteristics • Luminance: → 700cd/m^2 min. • Contrast ratio: → 450 min. • Luminance uniformity: → 1.2 typ. • Response time – Ton: (16)ms typ. → (17)ms typ. Toff: (16)ms typ. → (18)ms typ. • Note6: TopF = 30°C → TopF = 35°C **Signature of writer** *Approved by* *Checked by* *Prepared by* T. ITO R. KAWASHIMA